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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,553	06/20/2001	Lars-Peter Heineck	GR 98 P 1379 D	6319

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,553	HEINECK ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2002*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

Amendment A filed 08/29/2002 and entered as Paper No. 7 forms the basis of the present Office Action. In Amendment A Applicant canceled claim 2, incorporated claim 2 into claim 1 and substantially amended claim 1 by adding the further limitation "and having at least one side wall adjacent at least one of said conductive regions". All pending claims 1, 3-8 have thus been substantially amended either directly or indirectly through their dependence upon claim 1. Comments on Remarks made by Applicant in said Amendment A as given below in "Response to Arguments" are consequently limited to those aspects that are relevant to the present claim set.

Response to Arguments

1. Applicant's arguments filed 08/29/2002 have been fully considered but they are not persuasive. In particular, although Applicant's traverse of the objections are accepted, with some regret as to the readability of the specification, Applicant's allegation that the aforementioned further limitation now introduced into claim 1 is not shown by Sun et al: to wit, Sun et al show in Figure 19 the gate 6 to have at least one side wall (with region 23) adjacent at least one of said conductive regions 24. Furthermore, although Sun et al do finally remove the silicon nitride spacers, the rejection of the further limitation of old claim 2, now introduced into claim 1 as well, did not rely on the presence of nitride spacers in Sun et al, but instead relied upon the teaching of Ahmad in this regard. As to the allegation by Applicant that Ahmad does not

teach silicon nitride spacers Applicant is again referred to the abstract in Ahmad; see also column 4, lines 42-44. Applicant's allegation that 126 is not a real spacer as it lacks necessary thickness is unsubstantiated and irrelevant, since no thickness comparison is included, any thickness would have the effect of spacing and the function of the spacer comprises more than spacing, and in fact is aimed at producing the effects delineated in the previous office action, (and, parenthetically, in addition to being aimed at producing the slight Bird's Beak structure 124 underneath the gate near the corners of the gate) hence being an obvious improvement as explained. Therefore, the previous rejection needs essentially to be maintained at this time.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1 and 3-6*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al (5,612,249) in view of Ahmad (6,037,639).

With regard to claim 1: Sun et al teach (cf. Figure 19 and column 8, lines 40-53) a MOS transistor that may be used as a single-transistor memory cell, comprising: a semiconductor substrate 1 (cf. column 4, lines 50-52) having a substrate surface, a first conductive region and second conductive region (source and drain regions 24, see column 8, lines 48-52); a gate oxide 5/14 (cf. column 5, lines 24-33 and column 7, lines

12-27; note that the material constitution of regions 5 and 14 are prescribed in identical manner: both regions are to be made by oxidation of silicon; hence from the device point of view the regions 5 and 14 constitute a contiguous entity) disposed on said substrate surface; a gate 6/18 (cf. column 5, lines 34-37 and column 7, lines 65-67: note that regions 6 and 18 both materially are defined in exactly the same manner: they should consist of either poly or amorphous silicon; the distinction between gate 6 and interconnect 18 is thus from a device point of view moot, as both regions are materially identically specified and are, as gate and gate interconnect, required to have the same electrically conductive requirements) disposed on said gate oxide over an area between said first and second conductive regions (cf. Figure 19) and having at least one side wall (namely its interface with region 23), said sidewall being adjacent at least one of said conductive regions 24 (i.e., said sidewall between regions 5 and 23 is adjacent to region 24; and an insulating spacer 23 (cf. column 8, lines 40-43) disposed on said side wall of said gate, said spacer acting inherently as oxidation barrier (because material can burn only once); said gate oxide insulating said gate (note that the material constitution of the gate oxide is prescribed as the product of the oxidation of silicon, hence silicon oxide; see column 5, line 27; and column 7, lines 12-15) and having a thickened area below said side wall 23 of said gate.

Although Sun et al make use of nitride spacers in addition to oxide spacers, Sun et al do not necessarily specify the insulating spacer to be a silicon nitride spacer in the final structure. However, the use of nitride side wall spacers has long been recognized in the art of MOS transistors for the purpose of improving hot carrier resistance in ULSI

transistors, as evidenced by Ahmad (cf. abstract, column 1, lines 6-10, and column 2, lines 12-16, and column 4, lines 42-43). The higher dielectric constant of silicon nitride as compared to that of silicon oxide and its excellent barrier properties against hot carrier injection is amply elaborated in Ahmad (cf. column 4, lines 44-61).

Motivation to combine Ahmad's teaching of nitride side wall spacers with the invention of Sun et al is to improve hot carrier resistance for reduced transistor size. With a reduction of transistor size the electric field increases and hence improved protection is needed.

The invention can be easily *combined* by a simple replacement of the oxide spacers by nitride spacers, or, in the alternative, by retaining the silicon nitride spacers applied to the intermediate structure of Figure 15.

Reasonable expectation of success is justified because of the long-standing experience in the application of nitrogen implantation in silicon, and, in the alternative pertaining to the retainment of auxiliary silicon nitride spacers, only the omission of a step in the method of making would be necessary to achieve the same objective.

With regard to claim 3: said gate taught by Sun et al is specifically allowed to be include a layer of polysilicon (cf. column 5, lines 34-37 and column 7, lines 65-67). Therefore, the further limitation as defined in claim 3 does not distinguish over the prior art.

With regard to claim 4: Sun et al teach a layer of tungsten-silicide film 20 deposited on the polysilicon gate layer 18 (see Figure 17 and column 8, lines 13-18). Therefore, the primary reference teaches the further limitations defined by claim 4.

With regard to claim 5: said gate taught by Sun et al is specifically allowed to be include a layer of polysilicon (cf. column 5, lines 34-37 and column 7, lines 65-67).

With regard to claim 6: said gate taught by Sun et al is specifically allowed to include a tungsten silicide layer (column 8, lines 13-18 and Figure 17) and a polysilicon layer (cf. column 5, lines 34-37 and column 7, lines 65-67).

3. ***Claims 7-8*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al (5,612,249) and Ahmad (6,037,63) as applied to claims 6 and 1, respectively above, and further in view of Krautschneider ((5,854,500). As detailed above, claims 1 and 6 are unpatentable over Sun et al in view of Ahmad. Sun et al nor Ahmad necessarily teach the further limitation of claims 7 or 8. As shown by Krautschneider (front figure), however, lateral MOS transistors with attributes as essentially taught by the combination of the inventions of Sun et al and Ahmad, particularly with gate oxide 110 (see in Krautschneider column 5, lines 17-26 and column 6, lines 26-27) and nitride side spacers 114 (cf. column 6, lines 45-49), and with a gate of polysilicon (cf. column 5, lines 19-20) for instance have long been applied as selection transistors to DRAM memory cells (cf. abstract, first sentence), thus constituting an obvious use of said combinations of inventions.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

JPM
November 6, 2002